- ALU control lines (fis 4-2) - Data path timing (fis 4-3) - Steps - Control asistes set up - Registers are louded on to B bus - ALV and shifter opente - Results propasate on C bus back to reaster - Timing within a click cycle is implicit, timed by the propagation delay of the circuits

- Memory operations - 32-5it addressable memory port - Controlled by MAR (memory address register) and MDR (memory data resister) - Put the address of the word you want in MAR - Value is placed in MPR - &-bit layte-addressable wearing port - Controlled by PC resister, reads I byte into lower order lyte of MBR - MAR contains word addresses, PC contains light addresses . Putting a Z in PC and starting a memory read will read byte 2 four memory and put it in the low order lats of MBR - Putting a 2 in MAR and starting a memory read will read bytes 8-11 from menory and put them in MDR