Clocks

- Timing is important in many circuits
- A cluck is a circuit that emits pulses at regular intervals
- A clock's frequency is the number of pulses per second
 - The clock on a 4 GHz CPU has 4 billion pulses per second
 - Circuits with delays can be used to create subcycles
- Risag edge voltage switches from low to high (cutput from 0 to 1)
- Falling edge voltage surfiches from high to low (1 to 0)
- Output of the clock i's used as input to other circuits

Memory gades

- SR Latzh

- Two inputs

- S for setting the later (set to 1) - R For resetting the letch (set to 0)

- Two outputs Q and Q

- Not a combinational circuit

- Clocked SR latch

the latch can only change state when the clock is 1

- Clocked D latch

- A single input D and its complement are used as the S and R values

- when the clock is 1, D is street in the latch
- Avoids the possess of 5 and R being booth

- D flop-flop

- The change in state can only happen on the rising edge of the clock